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9. (Amended) A memory cell comprising:  
a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type; and  
a gate insulating layer formed over said substrate, the gate insulating layer having a first thickness formed over said first region and said second region, and a second thickness formed over said third region, said first thickness being greater than said second thickness; and  
an ONO stack formed on said gate insulating layer.

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10. (Amended) A method for fabricating a memory cell, the method comprising:  
providing a semiconductor substrate having a first region and a second region of one conduction type and a third region therebetween of an opposite conduction type;  
forming a first portion of a gate insulating layer over said first region and said second region; and  
etching said first portion of said gate insulating layer over said third region to form a second portion,  
said first portion having a first thickness said second portion having a second thickness, said first thickness being greater than said second thickness.

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Please cancel Claim 11.

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12. A method as in claim 10, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

Please add Claims 13-22.

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13. (New) A memory cell as in claim 8, wherein said first thickness is greater than said second thickness.

14. (New) A memory cell as in claim 8, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

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15. (New) A memory cell as in claim 8, wherein the electric field in a region of overlap between said gate insulating layer and said first and said second regions is between about 4 Mv/cm and 6 Mv/cm.

16. (New) A memory cell as in claim 8, wherein the electric field in a region of overlap between said gate insulating layer and said third region is between about 8 Mv/cm and 11 Mv/cm.

17. (New) (New) A memory cell as in claim 8, wherein said gate insulating layer comprises SiO<sub>2</sub>.

18. (New) A memory cell as in claim 9, wherein said first thickness is greater than said second thickness.

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19. (New) A memory cell as in claim 9, wherein said first thickness is between about 20 and 30 nm and wherein said second thickness is between about 8 and 11 nm.

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20. (New) A memory cell as in claim 9, wherein the electric field in a region of overlap between said gate insulating layer and said first and said second regions is between about 4 Mv/cm and 6 Mv/cm.

21. (New) A memory cell as in claim 9, wherein the electric field in a region of overlap between said gate insulating layer and said third region is between about 8 Mv/cm and 11 Mv/cm.

22. (New) A memory cell as in claim 9, wherein said gate insulating layer comprises SiO<sub>2</sub>.

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